IN THE SPECIFICATION

Please replace the paragraph at page 4, lines 4-13, with the following rewritten paragraph:

In the example of Figure 62, a source terminal (S) of the P-channel transistor 11a is designated as Vdd (power supply potential) and a cathode of the EL element 15 is connected to ground potential (Vk). On the other hand, an anode is connected to a drain terminal (D) of the transistor [[11b]] 11a. Besides, a gate terminal of the P-channel transistor [[11a]] 11b is connected to a gate signal line 17a, a source terminal is connected to a source signal line 18, and a drain terminal is connected to the storage capacitance 19 and a gate terminal (G) of the P-channel transistor 11a.

Please replace the paragraph at page 11, line 17, to page 12, line 11, with the following rewritten paragraph:

A twelfth invention of the present invention is an EL display apparatus comprising:

a display area where EL elements, driver transistors which supply light-emitting current to the EL elements, first switching elements which form paths between the driver transistors and the EL elements, and second switching elements which form paths between the driver transistors and source signal lines are formed in a matrix;

a first gate driver circuit which performs on/off control of the first switching elements;

a second gate driver circuit which performs on/off control of the second switching elements; and

~~a source driver circuit which applies video signals to the transistor elements; and~~

a source driver circuit which supplies programming current to the driver transistors,

wherein the driver transistors are P-channel transistors, and

transistors which generate the programming current in the source driver circuit are N-channel transistors.

Please replace the paragraph at page 43, line 20, to page 44, line 5, with the following rewritten paragraph:

Desirably, film thickness of the thin film is such that n·d is equal to or less than main emission wavelength λ of the EL element 15 (where n is the refraction factor of the thin film~~, or the sum of refraction factors~~ and d is the film thickness of the thin film); if two or more thin films are laminated, [[)]n·d of each thin film is calculated[[)]] and the results are summed ~~(d is the film thickness of the thin film, or the sum of refraction factors if two or more thin films are laminated)~~. By satisfying this condition, it is possible to more than double the efficiency of light extraction from the EL element 15 compared to when a glass substrate is used for sealing. Also, an alloy, mixture, or laminate of aluminum and silver may be used.

Please replace the paragraph at page 44, lines 6-25, with the following rewritten paragraph:

A technique which uses a thin encapsulation film 111 for sealing instead of a sealing lid 85 as described above is called thin film encapsulation. In the case of "underside extraction (see Figure 10; light is extracted in the direction of the arrow in Figure 10)" in which light is extracted from the side of the board 71, thin film encapsulation involves forming an EL film and then forming an aluminum electrode which will serve as a cathode on the EL film. Then, a resin layer is formed as a cushioning layer on the aluminum layer. An organic material such as acrylic or epoxy may be used for a cushioning layer. Suitable film thickness is from 1 μm to 10 μm (both inclusive). More preferably, the film thickness is from 2 μm to 6 μm (both inclusive). The encapsulation film [[74]] 111 is formed on the

cushioning film (layer). Without the cushioning film, structure of the EL film would be deformed by stress, resulting in streaky defects. As described above, the thin encapsulation film 111 may be made, for example, of DLC (diamond-like carbon) or an electrolytic capacitor of a laminar structure (structure consisting of thin dielectric films and aluminum films vapor-deposited alternately).

Please replace the paragraph at page 49, lines 10-21, with the following rewritten paragraph:

Preferably, the capacitor (storage capacitance) 19 should be from 0.2 pF to 2 pF both inclusive. More preferably, the capacitor (storage capacitance) 19 should be from 0.4 pF to 1.2 pF both inclusive. The capacity of the capacitor 19 is determined taking pixel size into consideration. If the capacity needed for a single pixel is Cs (pF) and an area (rather than an aperture ratio) occupied by the pixel is Sp (square μm), a condition $500/Sp \leq Cs \leq 20000/Sp$, and more preferably a condition $1000/Sp \leq Cs \leq 10000/Sp$ should be satisfied. Since gate capacity of the transistor is small, [[Q]] Cs as referred to here is the capacity of the storage capacitance (capacitor) 19 alone.

Please replace the paragraph at page 53, line 16, to page 54, line 2, with the following rewritten paragraph:

Incidentally, the gate of the transistor 11a and gate of the transistor 11c are connected to the same gate signal line [[11a]] 17a. However, the gate of the transistor 11a and gate of the transistor 11c may be connected to different gate signal lines [[11]] 17 (see Figure 32). Then, one pixel will have three gate signal lines (two in the configuration in Figure 1). By controlling ON/OFF timing of the gate of the transistor 11b and ON/OFF timing of the gate

of the transistor 11c separately, it is possible to further reduce variations in the current value of the EL element 15 due to variations in the transistor 11a.

Please replace the paragraph at page 68, lines 9-17 with the following rewritten paragraph:

According to the present invention, the source driver 14 is made of a semiconductor silicon chip and connected with a terminal on the source signal line 18 of the board 71 by ~~glass-on-chip~~ chip-on-glass (COG) technology. The source driver 14 can be mounted not only by the COG technology. It is also possible to mount the source driver circuit 14 by chip-on-film (COF) technology and connect it to the signal lines of the display panel. Regarding the driver IC, it may be made of three chips by constructing a power supply IC 82 separately.

Please replace the paragraph at page 70, lines 13-22 with the following rewritten paragraph:

The same applies to cases in which the source driver 14 is formed on the board 71 by polysilicon technology such as low-temperature polysilicon technology. A plurality of inverter circuits are formed between an analog switching gate such as a transfer gate which drives the source signal line 18 and the shift register of the source driver circuit 14. The following matters (shift register output and output stages which drive signal lines (inverter circuits placed between output stages such as output gates or transfer gates)) are common to the gate driver circuit and source driver circuit.

Please replace the paragraph at page 75, lines 15-21 with the following rewritten paragraph:

Incidentally, although it has been stated that the source driver IC 14 and gate driver IC 12 are made of silicon or other semiconductor wafers and mounted on the display panel, this is not restrictive. Needless to say, they may be formed directly on the display panel [[82]] 71 using low-temperature polysilicon technology or high-temperature polysilicon technology.

Please replace the paragraph at page 82, lines 1-9 with the following rewritten paragraph:

When input current is increased tenfold, output current is also increased tenfold, resulting in a tenfold increase in the EL brightness. Thus, to obtain predetermined brightness, a light emission period is reduced tenfold by reducing the conduction period of the transistor [[17d]] 11d in Figure 1 tenfold compared to a conventional conduction period. Incidentally, the tenfold increases/decreases are cited as an example to facilitate understanding and are not meant to be restrictive.

Please replace the paragraph at page 83, line 21, to page 84, line 4 with the following rewritten paragraph:

In white raster display, it is assumed that average brightness over one field (frame) period of the display screen 50 is B0. This drive method performs current (voltage) programming in such a way that the brightness B1 of each pixel 16 is higher than the average brightness B0. Also, a non-display area [[53]] 52 appears during at least one field (frame) period. Thus, in the drive method according to the present invention, the average brightness over one field (frame) period is lower than B1.

Please replace the paragraph at page 102, lines 10-20 with the following rewritten paragraph:

It is important to maintain terminal voltage of the capacitor 19. This is because ~~if~~ any change (charge/discharge) in the terminal voltage of the capacitor 19 ~~changes (charge/discharge)~~ during one field (frame) period~~, flickering occurs when the screen brightness changes and the frame rate lowers~~ causes changes in the screen brightness, resulting in flickering at lower frame rates. The current passed through the EL element 15 by the transistor 11a must be higher than 65%. More specifically, if the initial current written into the pixel 16 and passed through the EL element 15 is taken as 100%, the current passed through the EL element 15 just before it is written into the pixel 16 in the next frame (field) must not fall below 65%.

Please replace the paragraph at page 117, line 19, to page 118, line 4 with the following rewritten paragraph:

The shifting interval may be varied according to locations on the screen. For example, the shifting interval may be decreased in the middle of the screen, and increased at the top and bottom of the screen. For example, a pixel row may be shifted at intervals of 200 μsec. in the middle of the screen 50, and at intervals of 100 μsec. at the top and bottom of the screen 50. This increases emission brightness in the middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)[[)]]. Needless to say, the shifting interval is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Please replace the paragraph at page 118, lines 5-16 with the following rewritten paragraph:

Incidentally, the reference voltage of the source driver circuit 14 may be varied with the scanning location on the screen 50 (see Figure 146, etc.). For example, a reference current of 10 μA is used in the middle of the screen 50 and a reference current of 5 μA is used at the top of the screen 50. Varying a reference current in this way corresponding to a location in the screen 50, increases emission brightness in the middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)[[)]]. Needless to say, the reference current is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Please replace the paragraph at page 128, line 13, to page 129, line 2 with the following rewritten paragraph:

As shown in Figure 30, when the write pixel row is the (1)-th pixel row (see the 1H column in Figure [[30]] 31), the gate signal lines 17a(1), (2), (3), (4), and (5) are selected (in the case of configuration shown in Figure 1). That is, the switching transistors 11b and the transistors 11c in the pixel rows (1), (2), (3), (4), and (5) are on. Besides, since ISEL is low, the current output circuit A which outputs 25 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 130, lines 21-24 with the following rewritten paragraph:

Thus, each transistor 11a in the pixel row (1) deliver a current of Iw × 5 to the source signal line 18. Then, the capacitor 19 in ~~each~~ pixel row (1) is programmed with a 5 times larger current.

Please replace the paragraph at page 132, lines 11-20 with the following rewritten paragraph:

Besides, since ISEL is high, the current output circuit B which outputs 5 times larger current is selected and the current output circuit [[1222b]] B is connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b, which is in the same state as during the first 1/2 H. Thus, the switching transistors 11d in the pixel rows (2), (3), (4), (5), and (6) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 138, line 20, to page 139, line 9 with the following rewritten paragraph:

Figure 189 shows image display status in the first field. Figure 189(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current (voltage)). The location of the write pixel row is shifted in sequence: Figure 189(a1) → (a2) → (a3). In the first field, odd-numbered pixel rows are rewritten in sequence (image data in the even-numbered pixel rows are maintained). Figure 189(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 189(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 189(c). As can be seen from Figure 189(b), the EL elements 15 of the pixels in the odd-numbered pixel rows are non-illuminated.

On the other hand, the even-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 189(c) (N-fold pulse driving).

Please replace the paragraph at page 139, lines 10-24 with the following rewritten paragraph:

Figure 190 shows image display status in the second field. Figure 190(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current (voltage)). The location of the write pixel row is shifted in sequence: Figure 190(a1) → (a2) → (a3). In the second field, even-numbered pixel rows are rewritten in sequence (image data in the odd-numbered pixel rows are maintained). Figure 190(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 190(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 190(c). As can be seen from Figure 190(b), the EL elements 15 of the pixels in the even-numbered pixel rows are non-illuminated. On the other hand, the odd-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 190(c) (N-fold pulse driving).

Please replace the paragraph at page 141, line 18, to page 142, line 8 with the following rewritten paragraph:

The N-fold pulse driving method according to the present invention uses the same waveform for the gate signal lines 17b of different pixel rows and applies current by shifting the pixel rows at 1 H intervals. The use of such scanning makes it possible to shift illuminating pixel rows in sequence with the illumination duration of the EL elements 15 fixed to 1F/N. It is easy to shift pixel rows in this way while using the same waveform for the gate signal lines 17b of the pixel rows. It can be done by simply controlling data ST1 and ST2 applied to the shift register circuits 61a and 61b in Figure 6. For example, if Vg1 is

output to the gate signal line 17b when input ST1 is low and Vgh is output to the gate signal line 17b when input ST1 is high, ST2 applied to the shift register circuit [[17b]] 61b can be set low for a period of 1F/N and set high for the remaining period. Then, inputted ST2 can be shifted using a clock CLK2 synchronized with 1 H.

Please replace the paragraph at page 142, lines 9-20 with the following rewritten paragraph:

Incidentally, the EL elements 15 must be turned on and off at intervals of 0.5 msec or longer. Short intervals will lead to insufficient black display due to persistence of vision, resulting in blurred images and making it look as if the resolution has lowered. This also represents a display state of a data holding display. However, increasing the on/off intervals to 100 msec will cause flickering. Thus, the on/off intervals of the EL elements must be not shorter than 0.5 ~~μsec~~ msec and not longer than 100 msec. More preferably, the on/off intervals should be from 2 msec to 30 msec (both inclusive). Even more preferably, the on/off intervals should be from 3 msec to 20 msec (both inclusive).

Please replace the paragraph at page 143, lines 3-16 with the following rewritten paragraph:

Incidentally, it is preferable that the number of divisions of a black screen can be varied between still pictures and moving pictures. When N = 4, 75% is occupied by a black screen and 25% is occupied by image display. When the number of divisions is 1, a strip of black display which makes up 75% is scanned vertically. When the number of divisions is 3, three blocks are scanned, where each block consists of a black screen which makes up 25% and a display screen which makes up 25/3 percent. The number of divisions is increased for still pictures and decreased for moving pictures. The switching can be done either

automatically according to input images (detection of moving pictures) or manually by the user. Alternatively, the switching can be done according to input ~~outlet~~ content such as video on the display apparatus.

Please replace the paragraph at page 156, lines 4-12 with the following rewritten paragraph:

Thus, the gate signal line 17a is controlled by the gate driver circuit 12a while the gate signal line 17c is controlled by the gate driver circuit 12b. This makes it possible to freely specify the time to turn on the transistor 11b and reset the driver transistor 11a as well as the time to turn on the transistor [[111c]] 11c and program the driver transistor 11a with current. Other parts of the configuration are the same as or similar to those described earlier, and thus description thereof will be omitted.

Please replace the paragraph at page 159, penultimate line, to page 160, line 8 with the following rewritten paragraph:

Similarly, if the shift register circuit 61a outputs a high-level signal third, a turn-on voltage is output to the gate signal lines 17c of the pixel 16(2), which now is in a state of being programmed with current (voltage). At the same time, a turn-on voltage is also output to the gate signal lines 17a of the pixel 16(3), turning on the transistor 11b of the pixel 16(3) and resetting the driver transistor 11a of the pixel 16(3). Thus, the gate signal lines 17a outputs turn-on voltages for a period of 2 Hs, and the gate signal lines 17c receive a turn-on voltage for a period of 1 H.

Please replace the paragraph at page 161, lines 3-22 with the following rewritten paragraph:

As shown in Figure 39(a), the transistors 11c and 11e are turned off and the transistor 11d is turned on. Then, the drain (D) terminal and gate (G) terminal of the current-programming transistor [[11b]] 11a are short-circuited and a current Ib flows between them as shown in the figure. Generally, the transistor 11b has been programmed with current in the previous field (frame) and is capable of passing current (this is natural because the gate potential is held in the capacitor 19 for a period of 1F and image is displayed. However, current does not flow during a completely black display). In this state, as the transistor 11e is turned off and the transistor 11d is turned on, the drive current Ib flows through the gate (G) terminal of the transistor 11a (gate (G) terminal and the drain (D) terminal are short-circuited). Consequently, the gate (G) terminal and drain (D) terminal of the transistor 11a have the same potential, resetting the transistor 11a (to a state in which no current flows). Since the driver transistor 11b shares a common gate (G) terminal with the current-programming transistor 11a, the driver transistor 11b is also reset.

Please replace the paragraph at page 171, lines 3-11 with the following rewritten paragraph:

As in the case of Figure 33(a), if the reset mode in Figure 44(a) is synchronized with the voltage-programming mode in Figure 44(b), there is no problem because the period from the reset mode in Figure 44(a) to the current-programming mode in Figure 44(b) is fixed (constant). If this period is short, the driver transistors 11 are not reset completely. If it is too long, the driver transistor 11a is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen [[12]] 50 is decreased.

Please replace the paragraph at page 175, lines 10-16 with the following rewritten paragraph:

Thus, in the case of a QCIF display panel, which has 220 vertical scanning lines, at least 220/5 = 44 or more lines should be grouped into a block. More preferably, 220/10 = [[11]] 22 or more lines should be grouped into a block. However, if odd-numbered rows and even-numbered rows are grouped into two different blocks, there is not much flickering even at a low frame rate, and thus the two blocks are sufficient.

Please replace the paragraph at page 175, line 22 to page 176, line 5 with the following rewritten paragraph:

Incidentally, in the example in Figure 40, the gate signal lines 17b do not intersect the illumination control lines 401. Thus, there can be no defect in which a gate signal line 17b would become short-circuited with an illumination control line 401. Also, since there is no capacitive coupling between gate signal lines 17b and illumination control lines 401, ~~addition of capacitance~~ capacitive load is very small when the gate signal lines 17b are viewed from the illumination control lines 401. This makes it easy to drive the illumination control lines 401.

Please replace the paragraph at page 177, penultimate line, to page 178, line 2 with the following rewritten paragraph:

In the above example, one selection ~~pixel row~~ gate signal line is placed (formed) per pixel row. The present invention is not limited to this and a selection gate signal line may be placed (formed) for two or more pixel rows.

Please replace the paragraph at page 195, lines 16-19 with the following rewritten paragraph:

However, the present invention is not limited to this. The duration of the conduction period may be less than 1 H (1/2 H in Figure 197) as shown in Figure 197 or it may be equal to or ~~less~~ more than 1 H.

Please replace the paragraph at page 197, lines 5-12 with the following rewritten paragraph:

That is, when the gate driver circuit 12a outputs a turn-off voltage, the turn-off voltage is applied to the gate signal line 17a. When the gate driver circuit 12a outputs a turn-on voltage (logic low), it is ORed with the output of the OEV1 circuit by the OR circuit and the result is output to the gate signal line 17a. That is, when the OEV1 circuit is high, the turn-off voltage (Vgh) is output to the gate ~~driver~~ signal line 17a (see an exemplary timing chart in Figure 224).

Please replace the paragraph at page 198, lines 13-22 with the following rewritten paragraph:

Incidentally, screen brightness is adjusted under the control of OEV2. There are permissible limits to changes in screen brightness. Figure 223 illustrates relationship between permissible changes (%) and screen brightness (nt). As can be seen from Figure 223, relatively dark images have small permissible changes. Thus, in performing brightness adjustments of the screen 50 under the control of OEV2 or through duty cycle control, the brightness of the screen 50 should be taken into consideration. Permissible changes should be ~~shorter~~ smaller when the screen is dark than when it is bright.

Please replace the paragraph at page 203, lines 6-15 with the following rewritten paragraph:

The horizontal axis represents the ratio of the product of the reverse bias voltage Vm and its application duration t1 in a period to a rated terminal voltage V0. For example, if the reverse bias voltage Vm is applied at 60 Hz (60 Hz has no particular meaning) for 1/2 (half) a period, then t1 = 0.5. Further, t2 is the application duration of the rated terminal voltage. Also, if the terminal voltage (rated terminal voltage) is 8 V when a current with a current density of 100 A per square meter is applied at time 0 (zero) and if the reverse bias voltage Vm is [[8 V]] -8V, then |reverse bias voltage × t1|/(rated terminal voltage × t2) = |-8 (V) × 0.5|/(8 (V) × 0.5) = 1.0.

Please replace the paragraph at page 209, lines 5-17 with the following rewritten paragraph:

In the next 1 H (horizontal scanning period), a turn-off voltage (Vgh) is applied to the gate signal line 17a, and the second pixel row is selected. That is, a turn-on voltage is applied to a gate signal line 17b(2). On the other hand, a turn-on voltage (Vgl) is applied to the gate signal line 17b, the transistor 11d is turned on, and a current from the transistor 11a flows through the EL element 15, causing the EL element 15 to emit light. Also, a turn-off voltage ~~(Vsh)~~ (Vgh) is applied to the reverse bias line 471(1) stopping the reverse bias voltage from being applied to the EL elements 15 in the first pixel row (1). The voltage Vsl (reverse bias voltage) is applied to a reverse bias line 471(2) in the second pixel row.

Please replace the paragraph at page 216, lines 2-7 with the following rewritten paragraph:

To apply the reverse bias voltage Vm to the EL element 15, it is necessary to turn off the transistor 11a. To turn off the transistor 11a, the ~~Vdd~~ source terminal and gate (G) terminal of the transistor 11a can be short-circuited.

Please replace the paragraph at page 224, lines 11-20 with the following rewritten paragraph:

In particular, the present invention is characterized in that a first-stage current mirror circuit (current source 631) and second-stage current mirror circuits (current sources 632) are placed close to each other. If a first-stage current source 631 are connected with third-stage current sources 633 (i.e., in the case of two-stage current mirror circuit), the ~~second~~ third-stage current sources 633 connected to the first-stage current source are large in number, making it impossible to place the first-stage current source 631 and third-stage current sources 633 close to each other.

Please replace the paragraph at page 226, lines 8-16 with the following rewritten paragraph:

In the present invention, the terms "current sources 631, 632, and 633" and "current mirror circuits" are used interchangeably. That is, current sources are a basic construct of the present invention and the current sources are embodied into current mirror circuits. Thus, a current source is not limited to a current mirror circuit and may be a current circuit consisting of a combination of a operational amplifier 722, transistor [[631]] 631a, and register R as shown in Figure 72.

Please replace the paragraph at page 229, lines 10-18 with the following rewritten paragraph:

Incidentally, for ease of explanation, it is assumed that there are 63 current sources for a 6-bit configuration, but this is not restrictive. In the case of 8-bit configuration, 255 unit transistors 634 can be formed (placed). For a 4-bit configuration, 15 unit transistors 634 can be formed (placed). The transistors 634 constituting the unit current sources have a channel width W and channel ~~width~~ length L. The use of equal transistors makes it possible to construct output stages with small variations.

Please replace the paragraph at page 233, lines 5-16 with the following rewritten paragraph:

Kink effect occurs when the potential of the source signal lines 18 ~~vary~~ varies due to variations in Vt of driver transistors 11a shown in Figure 1 and the like. The driver circuit 14 passes programming current through the source signal line 18 so that the programming current will flow through the driver transistor 11a of the pixel. The programming current causes changes in the gate terminal voltage of the driver transistor 11a, and consequently the programming current flows through the driver transistor 11a. As can be seen From Figure 3, when a selected pixel 16 is in programming mode, the gate terminal voltage of the driver transistor 11a equals the potential of the source signal line 18.

Please replace the paragraph at page 234, lines 1-14 with the following rewritten paragraph:

Figure 118 is a graph which represents this phenomenon. The vertical axis represents the output current of the unit transistor 634 obtained when a predetermined voltage is applied

to the gate terminal. The horizontal axis represents the voltage between source (S) and drain (D). L in L/W represents the channel length and W represents the channel width of the unit transistor 634. Also, L, W represents the size of the unit transistor 634 which outputs current for one gradation. Thus, to output ~~with~~ the current for one gradation using a plurality of sub-unit transistors, W and L should be calculated by substituting the sub-unit transistors with an equivalent unit transistor 634. Basically, the calculation should be performed by taking into consideration the transistor size and output current.

Please replace the paragraph at page 239, line 19 to page 240, line 6 with the following rewritten paragraph:

Incidentally, it has been described that a voltage resistance process in the range of 2.5-V to 10-V (both inclusive) is used for the source driver IC [[12]] 14. This voltage resistance is also applied to examples (e.g., a low-temperature polysilicon process) in which the source driver circuit 14 is formed directly on an array board 71. Working voltage resistance of a source driver circuit 14 formed directly on an array board 71 can be high and exceeds 15 V in some cases. In such cases, the power supply voltage used for the source driver circuit 14 may be substituted with the IC voltage resistance illustrated in Figure 170. Also, the source driver IC 14 may have the IC voltage resistance substituted with the power supply voltage used.

Please replace the paragraph at page 240, lines 7-17, with the following rewritten paragraph:

The area of a unit transistor 634 is correlated with the variations in its output current. Figure 171 is a graph obtained by varying the transistor width W of a unit transistor 634 with the area of the unit transistor 634 kept constant. In Figure [[170]] 171, the variation of the unit transistor 634 with a channel width W of 2 μm is taken as 1. As can be seen from Figure

171 the variation rate increases gradually when W of the unit transistor is from 2 μm to 9 or 10 μm. The increase in the variation rate tends to become large when W is 10 μm or more. Also, the variation rate tends to increase when the channel width W = 2 μm or less.

Please replace the paragraph at page 240, lines 18-22, with the following rewritten paragraph:

In Figure 171, the permissible limit to the variation rate is 3 for 64- to 256-gradation display. The variation rate varies with the ~~area~~ shape of the unit transistor 634. However, the variation rate with respect to ~~the IC voltage~~ the channel width W resistance is hardly affected by the ~~area~~ shape of the unit transistor 634.

Please replace the paragraph at page 244, line 13, to page 245, line 8, with the following rewritten paragraph:

Terminal voltage of the resistor 691 provides a negative input to the operational amplifier 722 and the voltage at the negative terminal has the same magnitude as the voltage at a positive terminal of the operational amplifier 722. Thus, if a positive input voltage of the operational amplifier 722 is V1, the current obtained by dividing ~~with~~ this voltage by the resistance value of the resistance 691 flows through the transistor 1444. This current serves as the reference current. If the resistance of the resistor 691 is 100 KΩ and the input voltage of the positive terminal of the operational amplifier 722 is V1 = 1 (V), a reference current of 10 (μA) (= 1 (V)/100 KΩ) flows through the resistor 691. Preferably, the reference current is set between 2 μA and 30 μA (both inclusive). More preferably, it is set between 5 μA and 20 μA (both inclusive). A small reference current flowing through the parent transistor 63 lowers the accuracy of the unit current source 634. Too large a reference current increases the current mirror factor converted (in the downward direction in this case) within the IC,

increasing variations in the current mirror circuit, and thus lowering the accuracy of the unit current source 634 again.

Please replace the paragraph at page 246, penultimate line, to page 247, line 6, with the following rewritten paragraph:

The electronic regulator circuit 561 is built into the IC (circuit) 14. Alternatively, it is formed directly on an array board 71 using the low-temperature poly-silicon technology. A plurality of unit resistors (R1, R2, R3, R4, ... Rn) formed through polysilicon patterning are connected in series. Analog switches (S1, S2, [[S2]] S3, ... Sn+1) are placed among the unit resistors, the reference voltage Vref is divided, and the resulting voltages are output.

Please replace the paragraph at page 251, line 23, to page 252, line 8, with the following rewritten paragraph:

The current mirror factor of current sources may be varied (differed) from the other colors (from the current source circuits for the other colors) in an unfixed manner. It may be variable. The current mirror factor can be made variable by providing a plurality of transistors composing a current mirror circuit in a current source and changing, based on external signals, the number of transistors through which current ~~current~~ is passed. This configuration makes it possible to achieve an optimum white balance through adjustments while observing emission condition of manufactured EL display panels in various colors.

Please replace the paragraph at page 253, lines 4-18, with the following rewritten paragraph:

Figure 65 is an exemplary circuit diagram showing 176 outputs (N × M = 176) of a three-stage current mirror circuit. In Figure 65, the current source 631 constituted of the first-

stage current mirror circuit is referred to as a parent current source, the current sources 632 constituted of the second-stage current mirror circuits are referred to as child current sources, and the current sources 633 constituted of the third-stage current mirror circuits are referred to as grandchild current sources. The use of an integral multiple for the third-stage current mirror circuits which are the final-stage current mirror circuits makes it possible to minimize variations in the 176 outputs and produce high-accuracy current outputs. Of course, it should be remembered that the current sources [[531]] 631, 632, and 633 must be placed densely.

Please replace the paragraph at page 256, penultimate line, to page 257, line 6, with the following rewritten paragraph:

Thus, the configuration in which the unit transistor 634 in the output stage of the source driver IC (circuit) 14 is an N-channel transistor and the driver transistor 11a of the pixel 16 is a P-channel transistor is characteristic of the present invention. Incidentally, if all the transistors 11 composing the pixel 16 are ~~illustrated in Figure 1~~ P-channel transistors, this is more preferable because this can reduce the number of process masks required to produce the pixel 16.

Please replace the paragraph at page 262, line 22, to page 263, line 1, with the following rewritten paragraph:

It has been stated for ease of understanding and explanation that signals are transferred between current mirror circuits by way of voltage. However, by using current-based delivery. ~~It~~, it is possible to reduce variations in the driver circuit (IC) 14 of a current-driven display panel.

Please replace the paragraph at page 275, line 17, to page 276, line 10, with the following rewritten paragraph:

Figure 76 shows a configuration in which resistive elements 651 are formed (or placed) to control reference voltages of the three primary colors RGB independently. Of course, it goes without saying that the resistive elements 651 may be substituted with electronic regulators. Basic current sources including parent and child current sources such as the current source 631 and current sources 632 are placed densely ~~in~~ with an output current circuit 704 in an area illustrated in Figure 76. The dense placement reduces variations in outputs from the source signal lines 18. As illustrated in Figure 76, by placing them in the output current circuit 704 at the center of the source driver IC (circuit) 14, it becomes easy to distribute current to the left and right of the source driver IC (circuit) 14 from the current source 631 and current sources 632, resulting in reduced output variations between the left and right sides (it is all right to place them in a reference current generator circuit or controller instead of the current output circuit. That is, 704 is an area where an output circuit is not formed).

Please replace the paragraph at page 278, lines 6-10, with the following rewritten paragraph:

However, if transistors are connected in a one-to-one relationship with other transistors, any variation in the characteristics (Vt, etc.) ~~of characteristics~~ of a transistor will result in variations in the output of the corresponding transistor connected to it.

Please replace the paragraph at page 280, lines 1-5, with the following rewritten paragraph:

The use of multiple transistors for current-based delivery makes it possible to reduce variations in output current of the transistor group as a whole and further reduce variations ~~in~~ among the output current (programming current) of each terminal.

Please replace the paragraph at page 281, lines 6-15, with the following rewritten paragraph:

Now, description will be given of the relationship between the formation area of the transistor group 681 and the unit transistors 634. As also illustrated in Figure 66, a plurality of unit transistors 634 are connected per one transistor 633b. In the case of 64 gradations, 63 unit transistors 634 correspond to one transistor 633b (configuration in Figure 64). If the channel length L of the unit transistor [[633]] 634 is 10 μm and channel width W of the unit transistor 633 is 10 μm, the formation area Ts (square μm) of the unit transistor group is 10 μm × 10 μm × 63 = 6300 square μm.

Please replace the paragraph at page 282, lines 4-7, with the following rewritten paragraph:

~~Also, the~~The formation area Tmm of the transmission transistor group 681b and formation area Tms of the transmission transistor group 681c have the following relationship:

Please replace the paragraph at page 282, penultimate line, to page 283, line 13, with the following rewritten paragraph:

Incidentally, the above example is not limited to three-stage current mirror connections (multi-stage current mirror connections) shown in Figure 68. Needless to say, it is also applicable to single-stage current mirror connections. The example shown in Figure 123 involves connecting the transistor groups 681b (681b1, 681b2, 681b3, ...) each of which consists of multiple transistors 633a with the transistor groups 681c (681c1, 681c2, 681c3, ...) each of which consists of multiple transistors 633b. However, the present invention is not limited to this. It is also possible to connect a single transistor 633a with the transistor groups 681c (681c1, 681c2, 681c3, ...) each of which consists of multiple transistors 633b, or to connect the transistor groups 681b (681b1, 681b2, 681b3, ...) each of which consists of multiple transistors 633a with one transistor ~~group~~ 633b.

Please replace the paragraph at page 284, line 19, to page 285, line 8, with the following rewritten paragraph:

In the example shown in Figure 124, the adjustment transistors 1241 are placed, formed, or constructed at the 5th bit (the unit transistors 634 connected to the switch 641f) and 4th bit (the unit transistors 634 connected to the switch [[641d]] 641e). Four adjustment transistors 1241 each are placed or formed at the 5th bit and 4th bit. However, the present invention is not limited to this. The number of adjustment transistors 1241 for each bit may be changed. Also, adjustment transistors 1241 may be attached to all the bits (by forming, constructing, or placing them). The adjustment transistors 1241 are made smaller than the unit transistors 634. Alternatively, they are designed to produce smaller output current than

the unit transistors 634. Even if transistor size is fixed, it is possible to vary output current by varying W/L.

Please replace the paragraph at page 295, line 18, to page 296, line 2, with the following rewritten paragraph:

In the configuration shown in Figure 126, the current mirror circuit contains two or more (multiple) transistors 632a which pair with the transistors 633a. Since reference current are supplied from both sides, the gate terminal voltage of the transistors 633a is kept constant reliably in the transistor group [[681a]] 681b. Consequently, variations in the output current produced by the transistors 633a are extremely small. Thus, there are extremely small variations in the programming current outputted to the source signal line 18 or programming current drawn from the source signal line 18.

Please replace the paragraph at page 299, lines 18-24, with the following rewritten paragraph:

In Figure 129, ~~controls or adjusts~~ a reference current is controlled or adjusted by a reference current regulating means 651 (which, needless to say, is not limited to a variable regulator, and may be an electronic regulator). The unit transistors 634 form current mirror circuits in conjunction with the transistors 633b. The reference current Ib defines the magnitude of output current from the unit transistors 634.

Please replace the paragraph at page 300, lines 5-15, with the following rewritten paragraph:

However, there are often subtle differences between the gate terminal voltage of the unit transistors 634 in the transistor group 681c1 and the gate terminal voltage of the unit

transistors 634 in the transistor group 681c2. This is presumed to be due to voltage drops and the like caused by current flowing through the gate wiring and the like. Even a subtle change in voltage will result in a few percent change in output current (programming current). According to the present invention, difference among gradations is 1.5% (= 100/64) in the case of 64 gradations. Thus, changes in output current should be reduced to at least on the order of 1% or less.

Please replace the paragraph at page 301, line 17, to page 302, line 1, with the following rewritten paragraph:

Although two reference current generator circuits are formed separately in Figure 130, this is not restrictive and they may be constructed of the transistors 633a in the transistor group 681b shown in Figure 128. By using the configuration in Figure 128 and controlling (adjusting) the current passed through the transistors 632a composing current mirrors, it is possible to simultaneously control (adjust) the reference currents Ib1 and Ib2 shown in Figure [[130]] 128. That is, the transistors 633b1 and 633b2 are controlled as a transistor group (see Figure 130(b)).

Please replace the paragraph at page 305, lines 12-16, with the following rewritten paragraph:

In this way, the configuration in Figure 132 contains two transistors 633b which generate reference ~~current sources~~ currents. Figure 133 shows a configuration in which gate voltage of a transistor 633b2 constituting a reference current source is applied to the center of the common terminal 1253 as well.

Please replace the paragraph at page 309, line 18, to page 310, line 11, with the following rewritten paragraph:

Preferably, the total area Sc and the total area Sb are approximately equal. Also, it is preferably that the transistors 633a composing each transistor group 681b and the transistors 633b composing each transistor group 681c are equal in number. However, considering layout constraints on the IC chip 14, the transistors 633a composing each transistor group 681b may be made smaller in number and larger in size than the transistors 433b composing each transistor group 681c. An example of the above configuration is shown in Figure 157. The transistor group 681a consists of a plurality of transistors 632b. The transistor group 681a and transistors 633a compose a current mirror circuit. The transistors 633a generates current Ic. One transistor 633a drives a plurality of transistors 633b in a transistor group 681c (the current Ic from the single transistor 633a is shunted to the plurality of transistors 633b). Generally, the number of transistors 633a corresponds to the number of output circuits. For example, in a QCIF+ panel, there are 176 transistors 633a in each of R, G, and B circuits.

Please replace the paragraph at page 312, lines 3-6, with the following rewritten paragraph:

Incidentally, as illustrated in Figure 164, the transistor [[632a]] <u>632b</u> which forms current mirror circuits in conjunction with the transistor groups 681b does not need to be included in the transistor group 681a (see Figure 156).

Please replace the paragraph at page 316, lines 11-14, with the following rewritten paragraph:

Figure 151 illustrates potential fluctuations in the gate wiring 1261. ~~Linking~~ Blinking occurs at image change points (where the images change from white display to black display, from black display to white display, etc.).

Please replace the paragraph at page 323, lines 1-4, with the following rewritten paragraph:

As is the case with Figure 123, a plurality of transistors 633b may be provided to form a transistor group 681b1 and transistor group 681b2. Also, a plurality of transistors 633a may be provided to form a transistor group 681a as in Figure 123.

Please replace the paragraph at page 325, lines 14-23, with the following rewritten paragraph:

In Figure 213, the horizontal axis represents Sc × n/Sb and the vertical axis represents a fluctuation ratio. The fluctuation ratio in the ~~worst~~ best case is taken as 1. As illustrated in Figure 213, the fluctuation ratio deteriorates with increases in Sc × n/Sb. A large value of Sc × n/Sb means that the total area of the unit transistors 634 in the transistor groups 681c is larger than the total area of the transistors 633b in the transistor groups 681b when the number n of output terminals is constant. In that case, the fluctuation ratio is unfavorable.

Please replace the paragraph at page 326, lines 16-17, with the following rewritten paragraph:

Also, placement of unit transistors 634 in the transistor groups 681c ~~has~~ requires consideration.

Please replace the paragraph at page 328, line 18, to page 329, line 6, with the following rewritten paragraph:

Changes in the formation direction of the unit transistors 634 or sub-transistors 1352 often change their characteristics. For example, in Figure 135(c), ~~the unit transistor 634a~~ the sub-transistor 1352a and sub-transistor 1352b produce different output currents even if an equal voltage is applied to their gate terminals. However, in Figure 135(c), sub-transistors 1352 with different characteristics are formed in equal numbers. This reduces variations in the transistor (unit) as a whole. If the orientations of unit transistors 634 or sub-transistors 1352 with different formation directions are changed, differences in characteristics will complement each other, resulting in reduced variations in the transistor (single unit). Needless to say, the above items also apply to the arrangement in Figure 135(d).

Please replace the paragraph at page 329, last line, to page 330, line 16, with the following rewritten paragraph:

The above examples involve constructing or forming unit transistors of the same size or same current output in the transistor groups 681c (see Figure 139(b)). However, the present invention is not limited to this. A configuration illustrated in Figure 139(a) may also be used as follows. A single-unit unit transistor 634a is connected (formed) for the 0th bit (switch 641a). A 2-unit unit transistor 634b is connected (formed) for the 1st bit (switch

641b). A 4-unit unit transistor 634c is connected (formed) for the 2nd bit (switch 641c). An 8-unit unit transistor 634d is connected (formed) for the 3rd bit (switch 641d). A 16-unit unit transistor [[634a]] 634e is connected (formed) for the 4th bit (not shown). A 32-unit unit transistor [[634a]] 634f is connected (formed) for the 5th bit (not shown). Incidentally, a 16-unit unit transistor, for example, is a transistor which outputs current equivalent to the current outputted by 16 unit transistors 634.

Please replace the paragraph at page 331, lines 1-7, with the following rewritten paragraph:

Reference current circuits will be described below. Output current circuits 704 are formed (placed) individually for R, G, and B. The RGB output current circuits 704R, 704G, and 704B are placed in close vicinity. Also, a reference current INL in a low-current region in Figure 73 and reference current INH in a ~~low-current~~ high-current region in Figure 74 are adjusted to each color (R, G, and B) (see also Figure 79).

Please replace the paragraph at page 332, lines 8-13, with the following rewritten paragraph:

Output pads (output terminals) 761 are formed or placed on the output terminals of the IC chip. They are connected with the source signal lines 18 of the display panel. A bump is formed on the output pads 761 by a plating technique or ball bonding technique. The bump should be 10 to 40 μm high (both inclusive).

Please replace the paragraph at page 336, line 10, to page 337, line 8, with the following rewritten paragraph:

Figure 70 shows an example of a current-output type source driver circuit (IC) 14 equipped with a precharge function according to the present invention. Figure 70 shows a case in which the precharge function is provided in the output stage of a 6-bit constant-current output circuit. In Figure 70, a precharge control signal is constituted so that ~~it decodes the~~ it performs decoding in case ~~where~~ the higher order three bits D3, D4, and D5 in image data D0 to D5 are all zero by a NOR circuit 702, ~~takes an AND circuit 703~~ AND the results with an output from a counter circuit 701 of a dot clock CLK with a reset function based on a horizontal synchronization signal HD by an AND circuit 703, and thereby outputs a black level voltage Vp for a fixed period. In other cases, an output current from the current output stage 704 described with reference to Figure 68, etc. is applied to the source signal lines 18 (programming current Iw is drawn from the source signal lines 18). When the image data is composed of the 0th to 7th gradations close to the black level, by writing a voltage which corresponds to the black level only for a fixed period at the beginning of a horizontal period, the above configuration reduces the burden of current driving and makes up for insufficient writing. Incidentally, it is assumed that the 0th gradation corresponds to a completely black display while the 63rd gradation corresponds to a completely white display (in the case of 64-gradation display).

Please replace the paragraph at page 338, line 13, to page 339, line 6, with the following rewritten paragraph:

Incidentally, it is also useful to vary the precharge voltage and gradation range among R, G, and B because emission start voltage and emission brightness of EL elements 15 vary

among R, G, and B. For example, selective precharging is performed for 1/8 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the ~~01th~~ 0th to 7th gradations) in the case of R. In the case of other colors (G and B), selective precharging is performed for 1/16 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 0th to 3rd gradations). Regarding the precharge voltage, if 7 V is written into the source signal lines 18 for R, 7.5 V is written into the source signal lines 18 for the other colors (G and B). Optimum precharge voltage often varies with the production lot of the EL display panel. Thus, preferably precharge voltage is adjustable with an external regulator or the like. Such a regulator circuit can be also implemented easily using an electronic regulator circuit.

Please replace the paragraph at page 339, lines 7-9, with the following rewritten paragraph:

Incidentally, it is preferable that the precharge voltage is not higher than the anode voltage Vdd minus 0.5 V ~~and within~~ and not lower the anode voltage Vdd minus 2.5 V in Figure 1.

Please replace the paragraph at page 340, line 18, to page 341, line 1, with the following rewritten paragraph:

The precharge voltage PV is fed to an analog switch 731. To reduce on-resistance, the W (channel width) of the analog switch 731 should be 10 μm or above. However, it is set to 100 μm or below because too large W will increase parasitic capacitance as well. More preferably, the channel width W should be between 15 μm and 60 μm (both inclusive). The

above items also apply to the analog switch 731 in the switch [[641b]] 641a in Figure 75 and to the analog switch 731 in Figure 73.

Please replace the paragraph at page 344, lines 5-24, with the following rewritten paragraph:

Good results can also be obtained if the duration of application of the precharge voltage PV is varied using the image data applied to the source signal lines 18. For example, the application duration may be increased for the 0th gradation which corresponds to completely black display, and decreased for the 4th gradation. Also, good results can be obtained if the application duration is specified taking into consideration the difference between image data and image data to be applied 1 H later. For example, when writing a current into the source signal lines to put the pixels in black display mode 1 H after writing a current into source signal lines to put the pixels in white display mode, the precharge time should be increased. This is because a weak current is used for black display. Conversely, when writing a current into the source signal lines to put the ~~white~~ pixels in black display mode 1 H after writing a current into source signal lines to put the pixels in black display mode, the precharge time should be decreased or precharging should be stopped (no precharging should be done). This is because a large current is used for white display.

Please replace the paragraph at page 351, to page 352, line 7, with the following rewritten paragraph:

As described earlier, when the driver transistor 11a and selection transistors (11b and 11c) of the pixel 16 are P-channel transistors as shown in Figure 1, a penetration voltage is generated. This is because potential fluctuations of the gate signal line 17a penetrates to a terminal of the capacitor 19 via G-S capacitance (parasitic capacitance) of the selection

transistors (11b and 11c). When the P-channel transistor 11b turns off, the voltage is set to Vgh. As a result, the terminal voltage of the capacitor 19 shifts slightly to the Vdd side. Consequently, the gate (G) terminal voltage of the ~~selection~~ driver transistor 11a rises creating a more intense black display. This results in a proper black display.

Please replace the paragraph at page 364, lines 2-7, with the following rewritten paragraph:

Also, as shown in Figure 74, a reference current INH is applied to the high-current source circuit portion. Basically, this current serves as a unit current, a required number of unit transistors 634 operate according to input data H0 to [[L5]] H5, and the total current flows as a programming current IwH for the ~~low-current~~ high-current portion.

Please replace the paragraph at page 367, line 22, to page 368, line 15, with the following rewritten paragraph:

In the 5th and higher gradations, there is no change in the low-current region, i.e., (L0 to L4) = (1, 1, 0, 0, 1). In the high-current region, however, (H0 to H5) = (1, 0, 0, 0, 0) in the 5th gradation. Thus, a switch 641Ha turns on and one unit current source [[641]] 634 high-current region is connected to the source signal line 18. In the 6th gradation, (H0 to H5) = (0, 1, 0, 0, 0). Thus, a switch 641Hb turns on and two unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. Similarly, in the 7th gradation, (H0 to H5) = (1, 1, 0, 0, 0). Thus, two switches 641Ha and 641Hb turn on and three unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. In the 8th gradation, (H0 to H5) = (0, 0, 1, 0, 0). Thus, a switch 641Hc turns on and four unit current sources [[641]] 634 in the high-current region are connected to the source signal

line 18 as illustrated in Figure 84. Subsequently, switches 641 turn on and off in sequence and the programming current Iw is applied to the source signal line 18.

Please replace the paragraph at page 368, lines 16-24, with the following rewritten paragraph:

A feature of the above operations is that after the breakpoint, the programming current Iw applied to the high gradation part is composed of the current for the low gradation part plus a current which corresponds to each step (gradation) in the high gradation part. [[A]] At a change point of the low-current region and the high-current region, specifically, in the high-current region, for the programming current Iw, low current IwL is added. Therefore, the reference to "change point" may not be correct. A padding current IwK is also added.

Please replace the paragraph at page 371, line 21, to page 372, line 1, with the following rewritten paragraph:

In the 8th and higher gradations, there is no change in the low-current region, i.e., (L0 to L4) = (1, 1, 1, 0, 1). In the high-current region, however, (H0 to H5) = (1, 0, 0, 0, 0) in the 9th gradation. Thus, the switch 641Ha turns on and one unit current source [[641]] 634 in the high-current region is connected to the source signal line 18.

Please replace the paragraph at page 372, lines 2-16, with the following rewritten paragraph:

Similarly, the number of unit transistors 634 in the high-current region increases one by one with increasing gradation steps. Specifically, in the 10th gradation, (H0 to H5) = (0, 1, 0, 0, 0). The switch 641Hb turns on and two unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. Similarly, in the 11th gradation,

(H0 to H5) = (1, 1, 0, 0, 0). Two switches 641Ha and 641Hb turn on and three unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. In the 12th gradation, (H0 to H5) = (0, 0, 1, 0, 0). The switch 641Hc turns on and four unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. Subsequently, switches 641 turn on and off in sequence and the programming current Iw is applied to the source signal line 18 as illustrated in Figure 84.

Please replace the paragraph at page 373, lines 9-19, with the following rewritten paragraph:

Specifically, (L0 to L4) = (1, 0, 0, 0, 0) in the 1st gradation, (L0 to L4) = (0, 1, 0, 0, 0) in the 2nd gradation, (L0 to L4) = (1, 1, 0, 0, 0) in the 3rd gradation, and (L0 to L4) = (0, 0, 1, 0, 0) in the ~~2nd~~ 4th gradation. This continues to the 16th gradation. Specifically, (L0 to L4) = (1, 1, 1, 1, 0) in the 15th gradation and (L0 to L4) = (1, 1, 1, 1, 1) in the 16th gradation. In the 16th gradation, only the 5th bit (D4) out of D0 to D5 which represent gradations turns on, and thus it can be determined from the data signal line (D4) that the data D0 to D5 represent the 16th gradation. This reduces the hardware scale required for logic circuits.

Please replace the paragraph at page 373, line 20, to page 374, line 3, with the following rewritten paragraph:

The 16th gradation corresponds to a change point (breakpoint location). Rather, it ought to be said that the 17th gradation corresponds to a change point. In the 16th gradation, (L0 to L4) = (1, 1, 1, 1, 1) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, ~~four~~ five switches 641La, 641Lb, 641Lc, [[641d]] 641Ld, and 641Le in the low-current region turn on and 16 unit transistors 634 are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

Please replace the paragraph at page 374, lines 4-9, with the following rewritten paragraph:

In the 16th and higher gradations, there is no change in the low-current region, i.e., (L0 to L4) = (1, 1, 1, 0, 1). In the high-current region, however, (H0 to H5) = (1, 0, 0, 0, 0) in the 17th gradation. Thus, the switch 641Ha turns on and one unit current source [[641]] 634 in the high-current region is connected to the source signal line 18.

Please replace the paragraph at page 374, lines 10-22, with the following rewritten paragraph:

Similarly, the number of unit transistors 634 in the high-current region increases one by one with increasing gradation steps. Specifically, in the 18th gradation, (H0 to H5) = (0, 1, 0, 0, 0). The switch 641Hb turns on and two unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. Similarly, in the 19th gradation, (H0 to H5) = (1, 1, 0, 0, 0). Two switches 641Ha and 641Hb turn on and three unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18. In the 20th gradation, (H0 to H5) = (0, 0, 1, 0, 0). The switch 641Hc turns on and four unit current sources [[641]] 634 in the high-current region are connected to the source signal line 18.

Please replace the paragraph at page 377, lines 15-22, with the following rewritten paragraph:

As illustrated in Figure 87, the source driver circuit (IC) 14 according to the present invention consists of three current output circuits 704. They are a high-current-region current output circuit 704a which operates in a high current region, low-current-region current output

circuit 704b which operates in a low ~~and high~~ current ~~regions~~ region, and a ~~low-current-region~~ current-padding current output circuit [[704b]] 704c which outputs a padding current.

Please replace the paragraph at page 378, lines 4-15, with the following rewritten paragraph:

As also described earlier, the number of current output circuits 704 is not limited to three: the high-current-region current output circuit 704a, low-current-region current output circuit 704b, and current-padding current output circuit 704c. The source driver circuit (IC) 14 may consists of two current output circuits 704--the high-current-region current output circuit 704a and low-current-region current output circuit 704b--or ~~three~~ four or more current output circuits 704. Also, reference current sources 771 may be placed or formed for respective current output circuits 704 or a common reference current source 771 may be provided for all the current output circuits 704.

Please replace the paragraph at page 378, lines 23-29, with the following rewritten paragraph:

The current output circuits 704 respond to gradation data, and unit transistors 634 in them operate by drawing current from the source signal line 18. ~~Said and~~ The unit transistors 634 operate in sync with a horizontal ~~scanning period (1 H)~~ synchronization signal. That is, current is fed based on appropriate gradation data for a period of 1 H (if the unit transistors 634 are N-channel transistors).

Please replace the paragraph at page 389, lines 3-17, with the following rewritten paragraph:

If the common anode line 962 is 20 mm long, if wiring width is 150 μm, and if sheet resistance of the wiring is 0.05 Ω/□, the value of resistance is given by 20000 (μm)/150 (μm) × 0.05 Ω = approx. 7 Ω. If both ends of the common anode line 962 are connected to the base anode line 951 by a connection anode line 961c, the common anode line 962 is supplied with power from both sides, and consequently an apparent resistance value is 3.5 Ω (= 7 Ω/2). If this value is converted into a concentrated distribution ~~multiplier~~ constant, the apparent resistance value of the common anode line 962 is further halved and becomes 2 Ω or less. Even if anode current is 100 mA, a voltage drop in the common anode line 962 is 0.2 V or less. Furthermore, if the common anode line 962 and base anode line 951 are short-circuited by the connection anode line 961b in the center, there is almost no voltage drop.

Please replace the paragraph at page 397, lines 2-15, with the following rewritten paragraph:

Also, in Figure 99, the base anode line 951 and a cathode power line (base cathode line) 991 are laminated with an insulating film 102 placed between them. The laminate constitutes a capacitor. This architecture is referred to as an anode capacitor architecture. This capacitor functions as a power ~~path~~ bypass capacitor. Thus, sharp current changes in the base anode line 951 can be absorbed. If the display area of an EL display apparatus is [[S]] M square millimeters and the capacitance of a capacitor is C (pF), preferably the capacitance of the capacitor satisfies $M/200 \leq C \leq M/10$ or less. More preferably, it satisfies $M/100 \leq C \leq M/20$ or less. A small C makes it difficult to absorb current changes, but too large C makes the formation area of the capacitor too large and is not practical.

Please replace the paragraph at page 399, lines 10-24, with the following rewritten paragraph:

Figure 98 shows a sectional view taken along line [[a-a']] A-A' in Figure 99. In Figure 98(a), a source signal line 18 and connection anode line 961d of approximately the same width are laminated with an insulating film 102a placed between them. Preferably, the thickness of the insulating film 102a is between 500 and 3000 Angstrom (Å) both inclusive. More preferably, it is between 800 and 2000 Angstrom (Å) both inclusive. Small film thickness is not desirable because it will increase parasitic capacitance in the connection anode line 961d and source signal line 18 and tend to cause a short circuit between the connection anode line 961d and source signal line 18. On the other hand, thick film thickness will cause insulating-film formation to take time, resulting in long manufacturing time and high cost. Also, wiring on the upper side becomes difficult.

Please replace the paragraph at page 407, line 12, to page 408, line 6, with the following rewritten paragraph:

In the case of organic EL or other self-luminous elements, light produced by the EL elements 15 is reflected diffusely within the array board 71, causing intense light to be radiated from places other than the display screen 50. To prevent or reduce the diffusely reflected light, light-absorbing films 1011 are formed in ineffective areas which do not pass light effective for image display as illustrated in Figure 101 (on the other hand, effective areas are the display screen 50 and areas around it). The light-absorbing films are formed on an outer surface of a sealing lid 85 (light-absorbing film 1011a), inner surface of the sealing lid 85 (light-absorbing film 1011c), side face of the array board [[70]] 71 (light-absorbing film 1011d), area on the board other than the image display area (light-absorbing film

1011b), etc. Incidentally, instead of light-absorbing films, light-absorbing sheets or light-absorbing walls may be installed. Besides, the concept of light absorption also includes schemes or structures which diverge light by scattering it. In a broader sense, it also includes schemes or structures which confine light through reflection.

Please replace the paragraph at page 412, lines 12-19, with the following rewritten paragraph:

Thus, as illustrated in Figure 108, applied voltages of the gate driver circuit 12a are Vha (turn-off voltage for the gate signal line 17a) and Vla (turn-on voltage for the gate signal line 17a) while applied voltages of the gate driver circuit 12a are Vhb (turn-off voltage for the gate signal line 17b) and [[Vla]] Vlb (turn-on voltage for the gate signal line 17b). A relationship Vla < Vlb should be satisfied. Incidentally, Vha and Vhb may be approximately equal.

Please replace the paragraph at page 413, line 17, to page 414, line 2, with the following rewritten paragraph:

To generate the anode and cathode voltages of the EL elements 15 ~~of the gate driver circuits 12~~, the power supply IC 1091 needs to employ high voltage semiconductor processes. Such voltage resistance allows a level shift to signal voltage of the gate driver circuits 12. Also, as illustrated in Figure 205, level shifter circuits 2041 may be formed in the source driver IC 14. The level shifter circuits 2041 may be formed on left and right sides of the source driver IC 14. When using more than one source driver IC 14 as shown in Figure 205, one of the level shifter circuits 2041 in each source driver IC 14 is used.

Please replace the paragraph at page 420, lines 12-23, with the following rewritten paragraph:

Also, by using P-channel for the driver transistors (transistor 11a in Figure 1) which supply current to the EL element 15, it is possible to use a solid electrode made of thin metal film as the cathode of the EL elements 15. Also, current can be passed from the anode potential Vdd to the EL elements 15 in the forward direction. In view of the above circumstances, it is preferable that the transistors in the pixels 16 and gate driver circuits 12 are P-channel. Thus, the use of P-channel transistors as the transistors (driver transistors and ~~itching~~ switching transistors) in the pixels 16 and gate driver circuits 12 according to the present invention is not merely a design matter.

Please replace the paragraph at page 421, lines 8-24, with the following rewritten paragraph:

Incidentally, the level shifter circuit may be constructed from a semiconductor chip and mounted on the array board 71 using COG technology or the like. Also, the source driver circuit 14 is constructed basically from a semiconductor chip and mounted on the array board 71 using COG technology, as illustrated in Figure 109 and the like. However, this is not restricted to forming the source driver circuit 14 as a semiconductor chip and the source driver circuit 14 may be formed directly on the array board 71 using polysilicon technology. If P-channel transistors are used as the transistors 11 of pixels 16, programming current flows in the direction from the pixels 16 to the source signal lines 18. Thus, N-channel transistors should be used as the unit ~~current circuits~~ transistors (unit current sources) 634 of the source driver circuits (see Figures 73 and 74). That is, the source driver circuits 14 should be configured in such a way as to draw the programming current Iw.

Please replace the paragraph at page 430, lines 8-23, with the following rewritten paragraph:

It is important to take measures against heat generation from the EL display panel. As a measure against heat generation, a chassis 2062 made of metal material is mounted on the back of the panel (the side opposite to the illuminating surface of the display screen 50) as illustrated in Figure 206. For better heat dissipation, the chassis 2062 is provided with projections and depressions 2063. Also, a bonding layer is placed between the chassis [[2061]] 2062 and panel (the sealing lid 85 in the case of Figure 206). A material with good thermal conductivity is used for the bonding layer. Possible materials include, for example, silicone-resin paste and silicone paste. These materials are often used as an adhesive between a regulator IC and radiator plate. Incidentally, it is not strictly necessary for the bonding layer to have a bonding function as long as it serves the function of keeping the chassis [[2061]] 2062 and panel in intimate contact with each other.

Please replace the paragraph at page 431, lines 14-24, with the following rewritten paragraph:

Figure 208 illustrates a configuration of the display panel according to the present invention. A flexible board 84 is mounted on one side of the array board 71. A power supply circuit 82 ~~and the flexible board 84 are~~ is placed on the flexible board 84. Figure 209 shows a sectional view taken along line A-A' in Figure 208. However, in Figure 209, the flexible board 84 has been bent and the chassis 2062 has been mounted. As can be seen from Figure 209, the transformer 2011 of the power supply circuit 82 is contained in a space provided in the sealing lid 85. This makes it possible to reduce the thickness of the EL display panel (EL display panel module).

Please replace the paragraph at page 432, lines 17-25, with the following rewritten paragraph:

In addition to a push switch, the numeric key 572 may be a slide switch or other mechanical switch. Speech recognition may also be used for switching. For example, the switch may be configured such that display colors on the display screen 50 of the display panel will change as the user ~~speaks a phrase~~ enters a color change command by speaking such as "high-definition display," "4096-color mode," or "low-color display mode" into the phone. This can be implemented easily using existing speech recognition technology.

Please replace the paragraph at page 443, lines 8-18, with the following rewritten paragraph:

The pixel configuration in Figure 221 can perform N-fold pulse driving, duty cycle control driving, etc. if a peripheral circuit shown in Figure 222 is added. An image data signal is applied to the source signal line 18 from the video signal circuit 2212. A pixel 16 selection signal is applied to a selection signal line 2221 by an on/off control circuit 2215a, and consequently pixels 16 are selected one after another and image data is written into them. Also, an on/off signal is applied to an on/off signal line 2222 by an on/off control circuit 2215b, and consequently ~~the FED of pixels is~~ the pixels of the FED are subjected to on/off control (duty cycle control).